Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An integrated memory, comprising:

a memory cell array, the memory cell array having word lines for selecting memory cells and bit lines for reading out or writing data signals;

a read/write amplifier, the read/write amplifier being connected to the bit lines for assessing and amplifying data signals; and

a voltage generator circuit, including

a first capacitor,

a first transistor with a first terminal connected to an electrode of the first capacitor and a second terminal connected to a first supply potential,

a second transistor with a first terminal connected to the electrode of the first capacitor and a second terminal connected to a first terminal of the read/write amplifier, and

a pulse shaper connected to a control terminal of the first transistor and a control terminal of the second transistor, the pulse shaper controlling the first and second transistors such that the first transistor operates as an open switch and the second transistor operates as a closed switch for a predetermined period of time during an assessment and amplification operation of the read/write amplifier ~~for generating a voltage supply for application to the read/write amplifier, a potential difference being applied to the read/write amplifier using different supply potentials, the voltage generator circuit increasing the potential difference applied to the read/write amplifier for a limited period of time during an assessment and amplification operation of the read/write amplifier, wherein charge dependent control is implemented in the voltage generator circuit to generate the increased potential difference using a defined quantity of charge~~.

2. (Canceled)

3. (Currently Amended) The integrated memory as claimed in ~~claim 1~~ claim 6, wherein the voltage generator circuit has a first and a second supply path, the first supply path including the first and the second capacitors, and the first, second, third, and fourth transistors, and the second supply path including a fifth transistor with a first terminal connected to a third terminal of the read/write amplifier and a second terminal connected to a third supply potential and a sixth transistor with a first terminal connected to a fourth terminal of the read/write amplifier and a second terminal connected to a fourth supply potential, the fifth and sixth transistors controlled to operate as open switches for the predetermined period of time ~~two supply paths for the read/write amplifier, the supply paths having a different potential difference, the supply paths being driven alternatively to one another in time, the supply paths being connected to the read/write amplifier~~.

4. (Currently Amended) The integrated memory as claimed in claim 3, wherein an absolute value of a difference between the first supply potential and the second supply potential is greater than an absolute value of a difference between the third supply potential and the fourth supply potential ~~at least two capacitances, the capacitances connected into the supply path which has a higher potential difference, the capacitances being connected to a respective supply potential, the capacitances being connected to the read/write amplifier in the limited period of time, and the capacitances being discharged and charged in this state~~.

5. (Canceled)

6. (New) The integrated memory as claimed in claim 1, wherein the voltage generator circuit further includes

a second capacitor,

a third transistor with a first terminal connected to an electrode of the second capacitor and a second terminal connected to a second supply potential,

a fourth transistor with a first terminal connected to the electrode of the second capacitor and a second terminal connected to a first terminal of the read/write amplifier, and

the pulse shaper connected to a control terminal of the third transistor and a control terminal of the fourth transistor, the pulse shaper controlling the third and fourth transistors such that the third transistor operates as an open switch and the fourth transistor operates as a closed switch for the predetermined period of time.